2010-2011 ADCs Survey

ECE 627 Project

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Azadeh Zekri Esfahani

Contents:

Table I. List of 2010-2011 Published ADCs in Solid-State Circuits Conferences

	Conference	YEAR	TITLE	ABSTRACT	AUTHORS
1	ISSCC	2010	A Mostly Digital Variable-Rate Continuous-Time ADC ΔΣ Modulator	A mostly digital variable-rate continuous-time ΔΣ modulator is presented with power dissipation, output sample-rate, bandwidth, and peak SNDR ranges of 8 to 17mW, 0.5 to 1.15GHz, 3.9 to 18MHz, and 67 to 78dB, respectively. The IC is implemented in a 65nm CMOS process with an active area of 0.07mm2.	G. Taylor, I. Galton
2	ISSCC	2011	A 4Ghz cT ΔΣ adc with 70dB dR and -74dBFS Thd in 125Mhz Bw	A 4GHz CT ΣΔADC is presented with a loop filter topology that absorbs the pole caused by the input capacitance of its 4b quantizer and compensates for the excess delay caused by the quantizer's latency. Implemented in 45nm CMOS, the ADC achieves 70dB DR and -74dBFS THD in a 125MHz BW, while dissipating 256mW and occupying only 0.9mm2.	M. Bolatkale, L. Breems, R. Rutten, K. Makinwa
3	ISSCC	2011	An 8mw 50MS/s cT ΔΣ Modulator with 81dB SFdR and digital Background dac inearization	A 3rd-order single-loop CT ΔΣ modulator with a 4b quantizer is sampled at 500MHz with an OSR of 10. It achieves 63.5dB SNDR and -81dB SFDR in a 25MHz bandwidth without DEM. The DAC nonlinearity is digitally estimated and corrected. All feedback amplifiers are compensated for finite GBW influence. The modulator occupies 0.15mm2 in 90nm CMOS and achieves an FOM of 125fJ/conversion-step.	J. G. Kauffman, P. Witte, J. Becker, M. Ortmanns
4	ISSCC	2011	A Third-order dT ΔΣ Modulator using noise-Shaped Bidirectional Single-Slope Quantizer	A single-slope quantizer using modified bidirectional discharging is proposed. This quantizer provides first-order shaping of quantization noise and is used as the quantizer of a second-order delta-sigma loop. The fabricated prototype ADC achieves 78.2dB SNDR at 50MHz sampling speed at OSR of 24 with 2.9mW power consumption.	N. Maghari, U-K. Moon
5	ISSCC	2011	A 250mv 7.5µw 61dB SndR cMoS Sc ΔΣ Modulator using a near-Threshold-voltage-Biased cMoS inverter Technique	An ultra-low-voltage SC ΔΣ converter using a near-threshold-voltage-biasing technique is reported. This guarantees reliable operation of inverter-based integrators over temperature while running at a supply voltage of 250mV. An SNDR of 61dB is achieved for a BW of 10 kHz with a total power consumption of only 7.5µW.	F. Michel, M. Steyaert
6	ISSCC	2011	A 84dB SndR 100khz Bandwidth low-power Single op-amp Third-order ΔΣ Modulator consuming 140µw	A third-order ΔΣ modulator with single operational amplifier achieves 13.6 bits with 100kHz signal bandwidth and consumes 140µW. The time-interleaved two-integrators scheme is a modification of a second-order prototype. A slew-rate boost enables minimum power in a two stages op-amp. The SFDR is 96dB with an FoM of 54fJ/conversion-step.	A. Pena Perez, E. Bonizzoni, F. Maloberti
7	VLSI	2010	A 2.8-to-8.5mW GSM/Bluetooth/UMTS/DVB-H/WLAN Fully Reconfigurable CTΔΣ with 200kHz to 20MHz BW for 4G Radios in 90nm Digital CMOS	A 0.4mm2 low-power fully-reconfigurable continuous-time (CT) feedforward delta sigma ADC for 4G radios is implemented in 90nm CMOS. By reconfiguring the topology architecture, quantizer bits, biasing current and component parameters, optimal power consumption can be achieved for every mode. The modulator achieves a DR of 85/78/76/72/58dB for GSM/BT/UMTS/DVB-H/WLAN with 2.8/2.6/3.6/4.9/8.5mW from 1V supply. The FOM is 80.68/0.5/0.28/0.27/0.41pJ/conv.	Y. Ke, P. Gao, J. Craninckx*, G. Van der Plas*, G. Gielen, K.U. Leuven, Belgium, *IMEC, Belgium
8	VLSI	2010	A 2.8-to-8.5mW GSM/Bluetooth/UMTS/DVB-H/WLAN Fully Reconfigurable CTΔΣ with 200kHz to 20MHz BW for 4G Radios in 90nm Digital CMOS	A 0.4mm2 low-power fully-reconfigurable continuous-time (CT) feedforward delta sigma ADC for 4G radios is implemented in 90nm CMOS. By reconfiguring the topology architecture, quantizer bits, biasing current and component parameters, optimal power consumption can be achieved for every mode. The modulator achieves a DR of 85/78/76/72/58dB for GSM/BT/UMTS/DVB-	Y. Ke, P. Gao, J. Craninckx*, G. Van der Plas*, G. Gielen, K.U. Leuven, Belgium, *IMEC, Belgium

				H/WLAN with 2.8/2.6/3.6/4.9/8.5mW from 1V supply. The FOM is 0.68/0.5/0.28/0.27/0.41pJ/conv.	
9	VLSI	2010	A 2.8-to-8.5mW GSM/Bluetooth/UMTS/DVB-H/WLAN Fully Reconfigurable CTΔΣ with 200kHz to 20MHz BW for 4G Radios in 90nm Digital CMOS	A 0.4mm2 low-power fully-reconfigurable continuous-time (CT) feedforward delta sigma ADC for 4G radios is implemented in 90nm CMOS. By reconfiguring the topology architecture, quantizer bits, biasing current and component parameters, optimal power consumption can be achieved for every mode. The modulator achieves a DR of 85/78/76/72/58dB for GSM/BT/UMTS/DVB-H/WLAN with 2.8/2.6/3.6/4.9/8.5mW from 1V supply. The FOM is 0.68/0.5/0.28/0.27/0.41pJ/conv.	Y. Ke, P. Gao, J. Craninckx*, G. Van der Plas*, G. Gielen, K.U. Leuven, Belgium, *IMEC, Belgium
10	VLSI	2010	A 2.8-to-8.5mW GSM/Bluetooth/UMTS/DVB-H/WLAN Fully Reconfigurable CTΔΣ with 200kHz to 20MHz BW for 4G Radios in 90nm Digital CMOS	A 0.4mm2 low-power fully-reconfigurable continuous-time (CT) feedforward delta sigma ADC for 4G radios is implemented in 90nm CMOS. By reconfiguring the topology architecture, quantizer bits, biasing current and component parameters, optimal power consumption can be achieved for every mode. The modulator achieves a DR of 85/78/76/72/58dB for GSM/BT/UMTS/DVB-H/WLAN with 2.8/2.6/3.6/4.9/8.5mW from 1V supply. The FOM is 0.68/0.5/0.28/0.27/0.41pJ/conv.	Y. Ke, P. Gao, J. Craninckx*, G. Van der Plas*, G. Gielen, K.U. Leuven, Belgium, *IMEC, Belgium
11	VLSI	2010	A 2.8-to-8.5mW GSM/Bluetooth/UMTS/DVB-H/WLAN Fully Reconfigurable CTΔΣ with 200kHz to 20MHz BW for 4G Radios in 90nm Digital CMOS	A 0.4mm2 low-power fully-reconfigurable continuous-time (CT) feedforward delta sigma ADC for 4G radios is implemented in 90nm CMOS. By reconfiguring the topology architecture, quantizer bits, biasing current and component parameters, optimal power consumption can be achieved for every mode. The modulator achieves a DR of 85/78/76/72/58dB for GSM/BT/UMTS/DVB-H/WLAN with 2.8/2.6/3.6/4.9/8.5mW from 1V supply. The FOM is 0.68/0.5/0.28/0.27/0.41pJ/conv.	Y. Ke, P. Gao, J. Craninckx*, G. Van der Plas*, G. Gielen, K.U. Leuven, Belgium, *IMEC, Belgium
12	VLSI	2010	A 0.02mm² 65nm CMOS 30MHz BW All-Digital Differential VCO-Based ADC with 64dB SNDR	A 300MHz all-digital differential VCO-based ADC occupies 0.02mm² in 65nm CMOS, achieving a peak SFDR of 79dB and an SNDR of 64dB over a 30MHz BW. This high linearity is obtained using two VCOs in differential configuration in combination with an 11-points digital calibration. The power consumption is 11.4mW and the FOM is 150fJ/conv. step.	J. Daniels, W. Dehaene, M. Steyaert, Andreas Wiesbauer*, K.U. Leuven, Belgium, *Infineon Technologies, Austria
13	CICC	2010	82 dB SNDR 20-Channel Incremental ADC with Optimal Decimation Filter and Digital Correction	A third-order multi-channel incremental ADC with a 5-level quantizer is presented. An optimal decimation filter is used which minimizes the weighted sum of the thermal and quantization output noises. Digital correction is used to suppress mismatches in the multi-bit DAC. The prototype obtained a signal-to-noise-and-distortion ratio of 81.5 dB, within a total of 21.7 kHz signal bandwidth at a 10 MHz sampling frequency. The total power consumption for 20 channels is 6.7 mW	Wenhuan Yu1, Mehmet Aslan2 and Gabor C. Temes1
14	CICC	2010	A +5dBFS Third-Order Extended Dynamic Range Single-Loop ΔΣ Modulator	A new single-loop delta-sigma modulator with extended dynamic range is proposed. It employs an auxiliary multi-bit quantizer which processes the quantization error of the main quantizer. This addition guarantees improved stability over a wider input signal range. The cancelation of the quantization noise of the main quantizer is done via in-loop digital summation and is immune to opamp DC gain. As a proof of concept, a 3rd order modulator is designed in a 0.18µm CMOS process. This implementation incorporates a 3-level main quantizer, a 9-level auxiliary quantizer and 30dB open-loop opamp gain. Measurement results show that at 1.2V power supply and reference, the input signal can go over +5dBFS without any stability issues, achieving 75dB SNDR and 77.2dB dynamic range at OSR of 16. The clock frequency is 40MHz and the power dissipation is 4.9mW	Nima Maghari, Skyler Weaver and Un-Ku Moon

15	CICC	2010	A 63 dB 16 mW 20 MHz BW Double-Sampled ΔΣ Analog-to- Digital Converter with an Embedded-Adder Quantizer	A wideband ΔΣ ADC using a novel double-sampling scheme with a single set of capacitors and a dynamic embeddedadder quantizer is presented. The proposed quantizer eliminates static currents in the adder of a low-distortion architecture. Fabricated in 0.18 µm CMOS process, the prototype chip operates with a 320 MHz sampling frequency and achieves 63 dB SNDR in a 20 MHz signal band while consuming 16 mW power.	J. Chae1,3, S. Lee1, M. Aniya2, S. Takeuchi2, K. Hamashita2, P. K. Hanumolu1, and G. C. Temes1
16	CICC	2010	A 69.8 dB SNDR 3rd-order Continuous Time Delta-Sigma Modulator with an Ultimate Low Power Tuning System for a Worldwide Digital TV-Receiver	This paper presents a 3rd-order continuous time delta-sigma modulator for a worldwide digital TV-receiver whose SNDR is 69.8 dB. An ultimate low power tuning system using RC-relaxation oscillator is developed in order to achieve high yield against PVT variations. A 3rd-order modulator with modified single opamp resonator contributes to cost reduction by realizing very compact circuit. The mechanism to occur 2nd-order harmonic distortion at current feedback DAC was analyzed and a reduction scheme of the distortion enabled the modulator to achieved FOM of 0.18 pJ/conv-step.	Kazuo Matsukawa, Yosuke Mitani, Masao Takayama, Koji Obata, Yusuke Tokunaga, Shiro Sakiyama and Shiro Dosho
17	CICC	2010	A Robust STF 6mW CT ΔΣ Modulator with 76dB Dynamic Range and 5MHz Bandwidth	A third-order continuous-time delta-sigma modulator achieving 76dB dynamic range over 5MHz signal bandwidth is presented. The modulator has a monotonic lowpass signal transfer function and achieves over 70dB anti-aliasing. The prototype chip implemented in a 130nm CMOS process consumes 6mw power from a single 1.2V supply and occupies 0.56 mm2 active area.	Mohammad Ranjbar, Omid Oliaei and Robert W. Jackson
18	CICC	2010	A 5-MHz 11-bit Delay-Based Self-Oscillating ΣΔ Modulator in 0.025mm2	In this paper a self-oscillating ΣΔ modulator is presented. By introducing this self-oscillation in the system, the loop filter operates at a speed significantly lower than dictated by the clock frequency. This allows for a simple and power efficient design of the opamps used in the loop filter. The selfoscillation is induced here by introducing a controlled delay in the feedback loop of the modulator. A second order CMOS prototype was constructed in a 0.18 µm technology. A clock frequency of 850MHz generates a self-oscillation mode at 106.25 MHz. The modulator achieves a dynamic range (DR) of 66 dB for a signal bandwidth of 5 MHz. The power consumption is only 6mW and the chip area of the modulator core is 0.025mm2	Bart De Vuyst, Pieter Rombouts
19	ASSCC	2010	118-dB Dynamic Range, Continuous-Time, Opened-Loop Capactance to Voltage Converter Readout For Capacitive MEMS Accelerometer	A high performance analog front-end (AFE) interface circuit for capacitive MEMS accelerometer is presented in this paper. The AFE was implemented in a continuoustime (CT), chopper stabilized, capacitance to voltage converter (CVC) topology with a variable gain amplifier (VGA) for greater flexibility and a low pass filter (LPF) which limited the signal bandwidth to 300 Hz. Noise analysis of each building block of the AFE is also presented in this paper. The measured input referred noise density is 27 nV/ √ Hz. Long term stability results showed that the input offset has an Allan deviation floor of 60 nVrms. The nonlinearity for the AFE was measured at ± 1	Kevin T. C. Chai∗, Dong Han∗, Ravinder P. Singh∗, Duy D. Pham∗, Chin Y. Pang∗, Jian W. Luo∗, David Nuttman†, and Minkyu Je∗
20	ASSCC	2010	A 20MHz Bandwidth Continuous-Time Modulator with Jitter Immunity Improved Full-Clock Period SCR (FSCR) DAC and High Speed DWA	A 20MHz bandwidth continuous-time modulator with third-order active-RC loop filter and 4-bit quantizer is implemented in a 0.13 m CMOS process. The immunity to clock jitter is greatly improved by employing full clock period switched-capacitor-resistor (FSCR) DAC for feedback. A new data weighted averaging (DWA) technique is adopted to remove the timing bottleneck at 640MHz clock frequency. The modulator achieves 63.9dB peak-SNDR. Dynamic range is 68dB and decreases by only 2.3dB when RMS clock jitter is 15ps. The power consumption is 58mW from a 1.2V supply.	Jun-Gi Jo, Jinho Noh, and Changsik Yoo

21	ASSCC	2010	A 1.2V, 78dB HDSP ADC with 3.1V Input Signal Range	A low power, high resolution two-step hybrid deltasigma/ pipelined modulator (HDSP) is presented. The feedback architecture of the HDSP modulator is modified to allow higher orders of noise shaping. The pipelined quantizer is simplified. Finally, the input signal range of the HDSP modulator is extended beyond the supply voltage. The prototype chip is implemented in a 0.18µm CMOS process. With a 1.56 MHz bandwidth, 2.6 mW analog power consumption and 1.2 V analog supply voltage, the measured dynamic range and SNDR of this prototype IC are 78dB and 75dB.	O. Rajaee, S. Takeuchi1, M. Aniya1, K. Hamashita1, and U. Moon
22	ASSCC	2010	A 1V 350µW 92dB SNDR 24 kHz ΔΣ Modulator in 0.18µm CMOS	This paper presents a high precision multi-bit audio ΔΣ modulator working under 1V supply. We propose a kind of asynchronous 4-bit successive approximation quantizer without fast clock generation. Feed-forward topology with digital summing is adopted to relax the amplifier design requirement. Power efficient single stage OTA is adopted to drive the large sampling capacitor with low power consumption. Fabricated in 0.18µm standard CMOS, the modulator achieves 92dB SNDR with 24 kHz bandwidth and the power consumption is only 350µW. The active core die area is 0.64mm2.	Liyuan Liu1, Dongmei Li2, Liangdong Chen2, Chun Zhang1, Shaojun Wei1 and Zhihua Wang1
23	ASSCC	2010	A Low-Power Continuous-Time ΔΣ Modulator for Electret Microphone Applications	A continuous-time delta-sigma modulator that maybe used as an interface for Electret microphones is presented. The third order modulator comprises a single-ended-to-differential-converter integrated inside the loop-filter with a single-ended high-impedance input, an RC integrator on the first stage and Gm-C integrators for the other stages. Gm-C integrators comprise highly-linear low-power transconductances. The modulator has been designed and fabricated in the TSMC 0.18um technology for audio application (300Hz-10kHz) with a single supply voltage of 1.8V and a singleended input signal with a peak of 125mV. The measured dynamic range of the modulator is 86dB with a power consumption of 240uA.	Hashem Zare-Hoseini1,2, Izzet Kale2, and Richard C. S. Morling2
24	ASSCC	2010	A Regulator-Free 84dB DR Audio-Band ADC for Compact Digital Microphones	A 20kHz audio-band ADC with a single powersupply pad is implemented for a digital electret microphone. The designed low-noise preamplifier not only relaxes the ADC design requirement but also provides an excellent interface for the electret capacitor. A low power 4th-order switched-capacitor (SC) ΣΔ modulator (ΣΔM) converts the analog signal into 1b digital. Under the single power-supply pad, the switching noise effect on the signal quality is estimated via post simulations with simplified parasitic models. Performance degradation is minimized by time-domain noise isolation (TDNI) with sufficient time-spacing between the sampling edge and the output transition. A prototype ADC was implemented in a 0.18 m CMOS process. It operates under a minimum supply voltage of 1.6 V with total current of 420 µA. Operating at 2.56 MHz clock frequency, it achieves 84 dB dynamic range and a 64 dB peak signal-to-(noise + distortion) ratio. The measured power supply rejection at a 100 mVpp 217 Hz square wave is -72 dB without any supply regulation	Huy-Binh Le, Sang-Gug Lee, and Seung-Tak Ryu
25	ASSCC	2010	Power Optimization of High Performance Modulators for Portable Measurement Applications	In this paper, power optimization of two high performance modulators for portable measurement applications is presented. One modulator is a single-loop single-bit topology which achieves an 89.8dB peak SNDR	Jian Xu, Xiaobo Wu, Hanqing Wang and Junyi Shen, Bill Liu

				and consumes 20µW with a 1.5V supply. Here, a new power efficient current mirror Class-AB OTA is introduced to reduce the power. The other modulator adopts both multi-bit technique and switchedopamp (SO) technique to realize the ultra-low power target. Its total power consumption is only 9µW at a 1.8V supply, and the peak SNDR reaches 80.5dB. Especially, a new fully-clocked SO is proposed in this modulator to achieve a 50% power saving and double Figure-of-Merit (FOM) over the traditional type. Besides, to realize a zero-optimization coefficient of 1/100 and improve the performance, a novel resonator idea applicable to SO technique is adopted with 75% power and 70% area reduction. Both modulators are fabricated in a low cost 0.35µm CMOS process with a bandwidth of 1 kHz. The measured results show high FOM of the designed modulators.	
26	ESSCIRC	2010	A 0.13 µm CMOS 0.1-20MHz Bandwidth 86-70 dB DR Multi-Mode DT ADC for IMT-Advanced	This paper presents a reconfigurable tri-level/multibit multi-mode modulator implemented in 0.13 µm CMOS. The modulator covers between 0.1MHz and 20MHz signal bandwidth which makes it suitable for cellular applications including 4G radio systems, also known as IMT-Advanced. With a maximum sampling rate of 400MHz, the modulator achieves between 86 dB and 70 dB DR for 100 kHz and 20MHz signal bandwidth, respectively, at a scalable power consumption between 2mW and 34mW from a 1.2V supply, including the reference buffer	Thomas Christen1, Qiuting Huang
27	ESSCIRC	2010	A 100kHz-10MHz BW, 78-to-52dB DR,4.6-to-11mW Flexible SC ΣΔ Modulator in 1.2-V 90-nm CMOS	This paper presents an adaptive 1.2-V 90-nm CMOS cascade two-stage (2-2) SC ΣΔ modulator with 3-level quantization and unity signal transfer function in both stages. The chip reconfigures its loop filter order (either 2nd or 4th- order), clock frequency (from 40 to 240 MHz) and scales power according to the required specifications for different wireless standards, covering: GSM, Bluetooth, GPS, UMTS, DVB-H and WiMAX. Measurements feature a dynamic range of 78/70/71.5/66/62/52dB and a peak signal-to-(noise+distortion) ratio of 72.3/68.0/65.4/63.3 /59.1/48.7dB within 100kHz/500kHz/1MHz/2MHz/4MHz/10MHz, while consuming 4.6/5.35/6.2/8/8/11mW, respectively. These results show a competitive performance with the state-of-the-art multi-standard ΣΔ modulators, covering one of the widest regions in the DR-vs.-Bandwidth plane†	Alonso Morgado, Rocío del Río, Jose M. de la Rosa, Lynn Bos, Julien Ryckaert and Geert Van der Plas
28	ESSCIRC	2010	A Digitally Calibrated 5-mW 2-MS/s 4th-Order ADC in 0.25-µm CMOS with 94 dB SFDR	A digital calibration scheme is proposed to reduce the power consumption in a switched-capacitor (SC) ADC.When opamp bias current is reduced in the integrators, nonlinear settling errors dominate the output spectrum, causing harmonic distortion. The errors are detected using a parallel structure, and their effect is reduced by passing the post-filtered digital output through an inverse nonlinearity. With calibration, experimental results over a signal bandwidth of 1 MHz yield a peak signalto- noise-and-distortion ratio (SNDR) of 75 dB, a total harmonic distortion (THD) of −90 dB and a spurious-free dynamic range (SFDR) of 94 dB. The power dissipation of the calibrated modulator is 5 mW, a savings of 38% over a similarly performing uncalibrated ADC. The active area is 0.39 mm2 in 0.25-µm CMOS.	K. A. O'Donoghue, P. J. Hurst and S. H. Lewis
29	ESSCIRC	2010	A Configurable Cascaded Continuous-Time Σ Modulator with up to 15MHz Bandwidth	A reconfigurable cascaded continuous-time 3-1 Σ modulator with low PVT sensitivity was developed and implemented in 65nm digital CMOS. The 0.17mm2 chip achieves 67/55dB SNR and 70/61dB DR at 10/15MHz bandwidth with only 208MHz clock frequency and	Jens Sauerbrey, Jacinto San Pablo Garcia, Georgi Panov, Thomas Piorek, Xianghua Shen,

				10.5mW power consumption from a 1.3V supply.	Markus Schimper, Rudolf Koch
30	ESSCIRC	2010	A 0.08 mm2, 7mW Time-Encoding Oversampling Converter with 10 bits and20MHz BW in 65nm CMOS	This work presents an area- and power-efficient realization of a new Time-Encoding Oversampling Converter (TEOC) consisting of a 3rd-order CT loop filter and a selfoscillating PWM which displays similar performance than a standard multibit CT-ΣΔ modulator but has the complexity of a single bit design. The introduced Time-Encoding Quantizer (TEQ) is implemented inside a ΣΔ modulator by replacing a multibit quantizer. An innovative TEQ is used to overcome design issues in a 1.0V supply-voltage 65nm digital CMOS technology. The TEQ allows an exchange of amplituderesolution by time-resolution. The approach of time-resolution alleviates the scaling difficulties of mixed-signal circuits in nano-scale technologies. The TEOC features a 63dB dynamicrange and a peak-SNDR of 61dB over a 20MHz signal bandwidth. Clocked at 2.5GHz, the complete ADC consumes 7mW from a single 1.0V supply, including also the reference buffers. The ADC core results in an attractively small area of 0.08mm² and in a Figure-of-Merit (FoM=Pwr/2·BW·2ENOB) of 0.17pJ/conversion-step.	Enrique Prefasi1, Susana Paton1, Luis Hernandez1, Richard Gaggl2, Andreas Wiesbauer3, Joerg Hauptmann2

1. Table two (Performance survey of ADCs in Table one)

	ARCHITECTURE	TECHNOLOGY	AREA [mm^2]	SNDR [dB]	SNR [dB]	DR [dB]	SFDR [dB]	P [W]	fs [Hz]	OSR	BW [Hz]
[1]	VCO	0.065	0.07	77.8	80	77.8		1.70E-02	1.15E+09	128	4.50E+06
[2]	SDCT	0.045	0.9	65	65.5	70		2.56E-01	4.00E+09	16	1.25E+08
[3]	SDCT	0.09	0.15	63.5		70	81	8.00E-03	5.00E+08	10	2.50E+07
[4]	SDSC	0.18	0.44	78.2	79.3	78.2	86.3	2.90E-03	5.00E+07	24	1.04E+06
[5]	SDSC	0.13	0.34	61	64	61		7.50E-06	1.40E+06	70	1.00E+04
[6]	SDSC	0.18	0.49	84		88		1.40E-04	1.60E+06	16	5.00E+04
[7]	SDCT	0.09	0.4	82		85		2.80E-03	5.12E+07	128	2.00E+05
[8]	SDCT	0.09	0.4	76		78		2.60E-03	9.60E+07	96	5.00E+05
[9]	SDCT	0.09	0.4	75		75		3.60E-03	1.28E+08	32	2.00E+06
[10]	SDCT	0.09	0.4	72		72		4.90E-03	1.92E+08	24	4.00E+06
[11]	SDCT	0.09	0.4	58		58		8.50E-03	6.40E+08	16	2.00E+07
[12]	VCO	0.065	0.02	64		64	79	1.14E-02	3.00E+08	5	3.00E+07
[13]	INCR	0.18	6.25	81.5				3.40E-04	1.00E+07	230	2.17E+04
[14]	SDSC	0.18	0.85	75	76.1			4.90E-03	4.00E+07	16	1.25E+06
[15]	SDSC	0.18	0.35	63	63	64		1.60E-02	3.20E+08	8	2.00E+07
[16]	SDCT	0.18	0.09	69.8					1.40E+08	35	2.00E+06
[17]	SDCT	0.13	0.56	69.5	74.5	74.5		6.00E-03	1.60E+08	16	5.00E+06
[18]	SDCT	0.18	0.03	66				6.00E-03	8.50E+08	85	5.00E+06
[19]		0.18	7.6	118				1.20E-02			300
[20]	SDCT	0.13	1.17	63.9	65.7	68		5.80E-02	6.40E+08	16	2.00E+07
[21]	SDSC	0.18	3.79	75		78	87.5	6.35E-03	2.50E+07	8	1.56E+06
[22]	SDSC	0.18	0.64	92		94		3.50E-04	3.00E+06		2.40E+04
[23]	SDCT	0.18	0.33	78.2	81	86		2.42E-04			1.00E+04
[24]	SDSC	0.18	0.57	64		84		4.20E-04	5.00E+06		2.00E+04
[25]	SDSC	0.35		80	82.6	88		9.00E-06	3.20E+04		1.00E+03
[26]	SDSC	0.13	0.27	64.4	66.9	70.4	83.9	3.47E-02	4.00E+08		2.00E+07
[27]	SDSC	0.09	0.66	12.1bit		12.7bit		4.60E-03	1.20E+08		1.00E+05
[28]	SDSC	0.25	0.39	75			94	8.00E-03	6.20E+07		1.00E+06
[29]	SDCT	0.065	0.17	61	67	70	70	1.05E-02	2.08E+08		1.00E+07
[30]	SDCT	0.065	0.08	61				7.00E-03	2.80E+08		2.00E+07